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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank O'Mahony et al. Examiner: Ahmed Sefer
Serial No.: 09 893023 Group Art Unit: 2826
Filed: June 27, 2001 Docket: 884.405US1
Title: LOW LOSS INTERCONNECT STRUCTURE FOR USE IN MICROELECTRONIC CIRCUITS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. § 1.97(e)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. § 1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

FRANK O'MAHONY ET AL.

By their Representatives,

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By _____
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Date 29 April 2003

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 29 day of April, 2003.

Name

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